CLAIMS

Sub B1

1. A wave digital filter, comprising:

a plurality of memoryless adapters each having two or more ports, each port comprising an input and an output; and

at least one controlled gate which delays the propagation of a value into at least one input of at least one of the adapters.

C1

2. A filter according to claim 1, wherein the at least one controlled gate comprises at least one latch.

3. A filter according to claim 1, wherein the at least one controlled gate comprises at least one strobe gate.

4. A filter according to claim 1, wherein the at least one controlled gate is opened when the value it delays is expected to be valid.

5. A filter according to claim 1, wherein the value delayed by the at least one controlled gate is required with other values for performing a function and wherein the controlled gate is opened when all the values required for performing the function are expected to be valid.

6. A filter according to claim 1, wherein the at least one controlled gate is opened when substantially all the values entering the at least one of the adapters are expected to be valid.

7. A filter according to claim 1, comprising at least one delay unit which delays the propagation of a value into an input of one of the adapters for a predetermined time.

8. A filter according to claim 7, wherein the at least one delay unit comprises at least one controlled gate.

9. A filter according to claim 7, wherein the at least one delay unit comprises at least one uncontrolled delay element.

10. A filter according to claim 7, wherein the at least one delay unit delays the propagation of the value such that the value enters the one of the adapters substantially concurrently with another value received by the one of the adapters.

11. A filter according to claim 7, wherein the value whose propagation is delayed for the predetermined time comprises a valid value.

12. A filter according to claim 1, wherein at least one of the at least one controlled gate is located within one of the adapters.

13. A filter according to claim 1, wherein at least some of the plurality of adapters are three-port adapters.

14. A filter according to claim 1, wherein the value delayed from propagating into the adapter is received from a different adapter.

15. A filter according to claim 1, wherein the wave digital filter provides one or more results and wherein the at least one controlled gate does not affect the results provided by the wave digital filter.

16. A filter according to claim 1, wherein each of the at least one of the adapters into which propagation of values are delayed comprises at least one multiplier.

17. A filter according to claim 16, wherein each of the plurality of adapters comprises at least one multiplier.

18. A filter according to claim 1, wherein the plurality of adapters comprise at least two different types of adapters.

19. A filter according to claim 1, wherein the plurality of adapters comprise at least three different types of adapters.

20. A wave digital filter, comprising:

a plurality of memoryless adapters each having two or more ports, each port comprising an input and an output; and

at least one delay unit which delays the propagation of a first value into at least one input of at least one of the adapters such that the first value is received substantially concurrently with a second value at another input of the adapter.

21. A filter according to claim 20, wherein the at least one delay unit comprises a controlled gate.

22. A filter according to claim 20, wherein the at least one delay unit comprises an uncontrolled delay element.

23. A method of filtering a signal using a wave digital filter, comprising:

providing an input which carries a value required for performing a calculation by a memoryless adapter of the wave digital filter;

delaying the input until its value is valid; and

providing the valid value to the adapter.

24. A method according to claim 23, wherein providing the input comprises providing an input which carries a result from a different adapter.

25. A method according to claim 23, wherein delaying the input comprises delaying for a predetermined time.

26. A method according to claim 23, wherein delaying the input comprises delaying until all the values required for performing the calculation are expected to be valid.

27. A method according to claim 23, wherein delaying the input comprises delaying the input using a latch.

28. A method according to claim 23, wherein delaying the input comprises delaying the input using a strobe gate.

29. A method of filtering a signal using a wave digital filter, comprising:

providing a first input which carries a value required for performing a calculation by a memoryless adapter of the wave digital filter;

delaying the value on the first input until a valid value is received on a second input of the adapter; and

providing the delayed value to the adapter.

30. A method according to claim 29, wherein delaying the value on the first input comprises delaying for a predetermined time.

31. A method according to claim 29, wherein delaying the value on the first input comprises delaying the value using a latch.

32. A method according to claim 29, wherein delaying the value on the first input comprises delaying the value by an uncontrolled delay element.

33. A method of filtering a signal using a wave digital filter which includes a plurality of adapters, each adapter calculating a plurality of output values, comprising:

providing a clock signal to the filter; and

initiating calculation of one or more output values of a first group of less than all the adapters of the filter, responsive to the provided clock signal.

34. A method according to claim 33, wherein initiating calculation comprises initiating calculation of less than all the output values of the adapters of the first group.

35. A method according to claim 33, comprising initiating calculation of one or more output values of a second group of less than all the adapters of the filter, different from the first group of adapters, after termination of the calculation of the one or more output values of the adapters of the first group.

36. A method according to claim 35, wherein the first and second groups do not include common adapters.

37. A method according to claim 36, comprising initiating calculation of one or more additional output values of the adapters of the first group, different from the previously calculated output values of the first group, after calculating the one or more output values of the second group of adapters.

38. A method according to claim 37, wherein the calculation of the additional output values of the first group of adapters depends on at least one of the one or more output values of the second group of adapters.

39. A method according to claim 37, wherein the calculation of the output values of the second group of adapters depends on at least one of the one or more output values of the first group of adapters.

40. A method according to claim 33, wherein initiating calculation of output values of less than all the adapters comprises delaying input values into at least some of the adapters not included in the first group.

Add A1

Add B3

Add F1